Remarks

Claims 1-22 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

In the instant Office Action dated October 18, 2007, claims 1-22 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hiromoto (JP2001230375A).

Applicant respectfully traverses the § 102(b) rejection of claims 1-22 because the cited portions of the Hiromoto reference do not correspond to the claimed invention which includes, for example, aspects directed to a plurality of tilling structures. The Office Action misconstrues the cited portions of Hiromoto as corresponding to the claimed tilling structures. According to M.P.E.P. § 2111.01, the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification. In this instance, the cited portions of Hiromoto teach a ground shield (*see e.g.,* Figure 2 and Paragraphs 0063-0065 of Applicant's Specification), not tilling structures. More specifically, Hiromoto teaches that polysilicon 5b and metal silicide 8b form the 1st shielding pattern, which together with the 2nd shielding pattern (*i.e.,* metal silicide 8d) form a ground shield layer. *See, e.g.,* Figure 3a; paragraphs 0012, 0014 and 0036. Applicant submits that one of skill in the art would recognize that Hiromoto's ground shield does not correspond to the claimed tilling structures. *See, e.g.,* "A CMOS 10 GHz Voltage Controlled LC- Oscillator with integrated high-Q inductor", Wouter De Cock and Michiel Steyaert, Conference Esscirc 2001, proceedings p. 496-499; and Paragraphs 0004-0007 of Applicant's Specification. More specifically, Applicant's specification states that tilling structures (as is known in the art) are used to increase or decrease the pattern density in empty or large metal layers respectively in order to improve the manufacturability of the semiconductor device. *See, also,* U.S. Patent No. 7,152,215, Col. 1:54-59. In contrast, Hiromoto's ground shield layer is used to prevent coupling between an inductor and a substrate. *See, e.g.,* Figure 3a of Hiromoto; and Figure 2 and Paragraphs 0063-0065 of Applicant's Specification. As such, Hiromoto's ground shield layer is not taught to increase or decrease the pattern density for manufacturability. Accordingly, Applicant submits that the Office Action's assertion that Hiromoto's ground shield corresponds to Applicant's tilling structures is inconsistent

with the meaning of a tilling structure as defined by Applicant's specification, which differentiates a ground shield from tilling structures.

Moreover, the claims have been amended to explicitly recite limitations that the skilled artisan would have recognized as being implicit to a tilling structure (*i.e.,* that tilling structures are arranged or provided to improve manufacturability of the semiconductor device). Therefore, Applicant submits that these amendments are not intended to change the scoped of the claims. Applicant further submits that the Hiromoto does not teach or suggest that the 1st shielding pattern is arranged or provided to improve manufacturability of a semiconductor device.

In view of the above, the cited portions of Hiromoto do not correspond to the claimed tilling structures. Accordingly, the § 102(b) rejection of claims 1-22 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claim 4 because the cited portions of Hiromoto do not correspond to aspects of the claimed invention directed to the geometrical pattern of tilling structures at two different layers being different in shape and/or orientation. The Office Action improperly asserts that Hiromoto's polysilicon 5b and metallic silicate 8b are different in shape and/or orientation. The cited portions of Hiromoto clearly teach that polysilicon 5b and metallic silicate 8b each have the same shape and orientation (*i.e.,* metallic silicate 8b is formed on top of polysilicon 5b), with polysilicon 5b and metallic silicate 8b forming the 1st shielding pattern. *See, e.g.,* Figures 1b and 3; paragraph 0012. Accordingly, the § 102(b) rejection of claim 4 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claim 8 because the cited portions of the Hiromoto reference do not correspond to aspects of the claimed invention directed to the tilling structures being a plurality of substantially triangular elements. Hiromoto does not teach that polysilicon 5b and metallic silicate 8b are formed of substantially triangular elements. *See, e.g.,* Figures 1a, 1b and 3. Accordingly, the § 102(b) rejection of claim 8 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 15-16 because the cited portions of Hiromoto do not correspond to aspects of the claimed invention directed to a further passive element. The cited portions of the Hiromoto reference do not

mention a further passive element, let alone that the further passive element is a capacitor. *See, e.g.,* Figure 3, paragraph 0036, and the Abstract. These portions of Hiromoto discuss the parasitic capacitance between the inductor and the 1st and 2nd shield patterns, not that the device includes a separate passive element (*e.g.,* a capacitor). Applicant submits that one of skill in the art would recognize that a parasitic capacitance is not equivalent to a separate capacitive element as in the claimed invention. Moreover, the purpose of the Hiromoto reference is to reduce this parasitic capacitance. *See, e.g.,* paragraph 0036. Accordingly, the § 102(b) rejection of claims 14-15 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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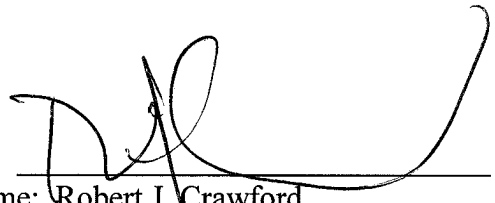
By: 
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